What is claimed is:

1. A sampling circuit for an analog signal according to a clock signal, comprising:

a first thin film transistor (TFT), having a first electrode to receive the analog signal, a control electrode to receive the clock signal and a second electrode for sampling the analog signal when the clock signal is at a first logic level; and

a counteracting device coupled to the second electrode, wherein when the clock signal is changed from the first logic level to a second logic level, feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT is reduced.

2. The circuit as claimed in claim 1, wherein the counteracting device is a capacitor between the second electrode and a reference potential node.

3. The circuit as claimed in claim 1, wherein the counteracting device comprises an inversion device, having an input terminal coupled to the control electrode, and a capacitor between the second electrode and a output terminal of the inversion device.

4. The circuit as claimed in claim 3, wherein the capacitor comprises a second TFT having a gate terminal coupled to the output terminal of the inversion device

and a source and drain terminal both coupled to the second electrode.

5. A liquid crystal display, comprising:

a plurality of display units, arranged in array;

a plurality of data lines disposed corresponding to each line of the display units, wherein each data line provides a video signal to the corresponding display unit; and

a data driving circuit, having at least one sampling circuit, sampling an image signal to be the video signal according to a clock signal, and the sampling circuit comprising:

a first thin film transistor (TFT), having a first electrode receiving an analog signal, a control electrode receiving the clock signal, and a second electrode for sampling the analog signal when the clock signal is at a first logic level; and

a counteracting device coupled to the second electrode, wherein when the clock signal is changed from the first logic level to a second logic level, a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT is reduced.

6. The liquid crystal display as claimed in claim 5, wherein the counteracting device is a capacitor

between the second electrode and a reference potential node.

7. The liquid crystal display as claimed in claim 5, wherein the counteracting device comprises an inversion device, whose input terminal is coupled to the control electrode, and a capacitor between the second electrode and an output terminal of the inversion device.

8. The liquid crystal display as claimed in claim 7, wherein the capacitor comprises a second TFT having a gate terminal coupled to the output terminal of the inversion device and a source and drain terminal, both coupled to the second electrode.